

# Echelle diffraction grating based high-resolution spectrometer-on-chip on SiON waveguide platform

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An echelle diffraction grating based high-resolution spectrometer-on-chip on silicon oxynitride (SiON) waveguide platform operated at a wavelength range of 850 nm is demonstrated. The chip comprises 120 output waveguides with 0.25-nm wavelength channel spacing and has a size of only  $11 \times 6$  (mm). The experimental results show that the insertion loss is  $-14$  dB, the measured adjacent channel crosstalk is less than  $-25$  dB, the 3 dB channel bandwidth is  $< 0.1$  nm, and the channel non-uniformity is 3 dB for 56 channels with a wavelength ranging from 838 to 852 nm.

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With the advancement of the wavelength-division multiplexing systems in optical communication in the past two decades, two types of planar waveguide based grating devices have been developed, namely, arrayed waveguide grating (AWG) and echelle diffraction grating (EDG). Recently, the application of AWG and EDG in the sensing area has received substantial interest because of their powerful ability in high-resolution spectral analysis with compact size, and potential for on-chip multi-functional integration<sup>[1,2]</sup>. High index contrast silicon-on-insulator platform has been chosen for planar waveguide devices working above 1100 nm<sup>[3,4]</sup>, which is the absorption edge of silicon, whereas the silicon oxynitride (SiON) waveguide platform for wavelength range below 1100 nm is favorable because of its variable refractive index (from 1.47 to 2.3) and broad highly transparent wavelength range (210 nm to 2000 nm)<sup>[5]</sup>. SiON waveguide based AWG spectrometers have been recently reported, especially for Raman spectroscopy<sup>[6]</sup> and optical coherence tomography<sup>[7,8]</sup>. Compared with AWG, EDG is significantly smaller because a folded beam path is used. The current study presents a SiON waveguide based EDG spectrometer-on-chip operating in a wavelength range of 850 nm.

Figure 1 shows the schematic of our EDG device. Through the input waveguide, light arrives at the boundary of the slab waveguide, diverges into the slab waveguide, illuminates the echelle grating facets, diffracts back, and then converges to the designated output waveguide according to its wavelength.

The channel waveguide ( $1.25 \mu\text{m}$  wide and  $1 \mu\text{m}$  high) was chosen as the core waveguide structure for the input and output waveguides. Single-mode operation around 850 nm is achieved with the refractive index of 1.52 for the SiON core layer and 1.46 for the  $\text{SiO}_2$  buffer and upper cladding layers. The adjacent output waveguides are separated by a gap of  $2.75 \mu\text{m}$  to minimize crosstalk. This gap corresponds to an output waveguide spacing of  $4 \mu\text{m}$ , which is spread out to  $32 \mu\text{m}$  via curved waveguides. Considering the wavelength channel spacing of 0.25 nm, a linear dispersion coefficient of 16 000 is obtained. The total number of output waveguides is 120,

and the EDG was designed with a free spectral range of 28 nm at the 30th diffraction order. The number of grating teeth is 600, which is large enough to cover more than 99% of light energy emitted from the input waveguide. The average facet size of the grating teeth is  $8 \mu\text{m}$ . The total size of the designed EDG chip is  $11 \times 6$  (mm). Compared with the SiON based AWG with similar performance at around 800 nm proposed by He *et al.*<sup>[9]</sup>, the size of the designed EDG is eight times smaller than the AWG, proving the size reduction caused by folded beam path in EDG. The two-stigmatic-point method was used to design the grating structure, and the scalar diffraction theory was performed to simulate and to optimize the device<sup>[10,11]</sup>.

The device was fabricated on a polished silicon wafer. Plasma-enhanced chemical vapor deposition (PECVD), with a basic operating environment at a temperature of  $300^\circ\text{C}$ , a working pressure of 300 Pa, and a 13.56 MHz radio frequency power of 700 W was used to conduct film deposition. First, a  $6\text{-}\mu\text{m}$   $\text{SiO}_2$  buffer layer was deposited at a deposition rate of  $0.15 \mu\text{m}/\text{min}$  using  $\text{SiH}_4$  and  $\text{N}_2\text{O}$ ,

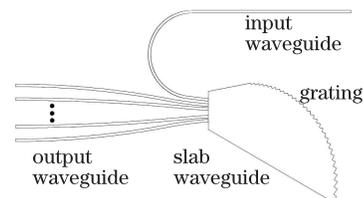


Fig. 1. Schematic of EDG.

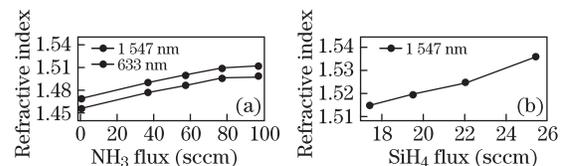


Fig. 2. (a) Refractive index variation of the SiON layer with the  $\text{NH}_3$  flux when the  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  fluxes are fixed at 20 and 350 sccm, respectively, measured at 1547 and 633 nm; (b) refractive index variation of the SiON layer with the  $\text{SiH}_4$  flux when the  $\text{NH}_3$  and  $\text{N}_2\text{O}$  fluxes are fixed at 190 and 350 sccm, respectively, measured at 1547 nm.

with gas fluxes of 20 and 2000 sccm, respectively. Such thickness is sufficient to prevent the light from leaking to the silicon substrate. Subsequently, 1- $\mu\text{m}$  SiON core layer was deposited with  $\text{SiH}_4$ ,  $\text{N}_2\text{O}$ , and  $\text{NH}_3$ . The refractive index of SiON has a wide tuning range; thus, carefully tuning the ratio of the three gas fluxes is necessary to obtain the required refractive index. After a large number of attempts and adjustments, the gas fluxes of  $\text{SiH}_4$ ,  $\text{N}_2\text{O}$ , and  $\text{NH}_3$  were fixed to 17.5, 350, and 190 sccm, respectively, to achieve a deposition rate of 0.4  $\mu\text{m}/\text{min}$  and a refractive index of 1.52. A positive refractive index uniformity of 0.001 was measured using the prism coupler method on a 4-inch wafer. The refractive index of the SiON layer increased with the  $\text{NH}_3$  flux for fixed  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  fluxes, as well as with the  $\text{SiH}_4$  flux for fixed  $\text{NH}_3$  and  $\text{N}_2\text{O}$  fluxes, as shown in Figs. 2(a) and (b), respectively. After SiON film formation, another 1.5- $\mu\text{m}$   $\text{SiO}_2$  upper cladding film was deposited under the same condition as the buffer layer.

The formation of a vertical and smooth sidewall is important for the grating teeth during the deep-etching step to achieve a high performance EDG chip in terms of insertion loss and adjacent channel crosstalk. Figure 3 shows the excess loss caused by the slope angle of the grating facet for our SiON waveguide structure, which was calculated with the scalar diffraction method. A slope angle deviation of less than  $3^\circ$  from the vertical is necessary to limit the excess loss below 1 dB.

The common method for etching  $\text{SiO}_2$  and SiON waveguides is to use  $\text{CHF}_3/\text{CF}_4$  inductively coupled plasma (ICP) etching with photoresist mask. However, our experiments showed that this process resulted in a sidewall angle deviation of about  $5^\circ$  from the vertical, significantly degrading the performance of the EDG chip. Two measures were taken to improve the sidewall verticality. One measure uses chromium metal hard mask to replace the photoresist to increase the etching selectivity from 1:2 to 1:100, whereas the other measure tunes the gas ratio of  $\text{CHF}_3$  and  $\text{CF}_4$  to balance the etching and the sidewall protecting mechanism during the ICP etch process<sup>[9]</sup>.

The chromium hard mask was formed by sputtering 150-nm-thick chromium film onto the  $\text{SiO}_2$  upper cladding layer via a magnetron sputtering machine. Subsequently, a 500-nm-thick  $\text{SiO}_2$  film was deposited by PECVD, and used as the etching mask for chromium etching. A 1.3- $\mu\text{m}$ -thick AZ5214E positive photoresist was spun onto the  $\text{SiO}_2$  film, exposed, and then

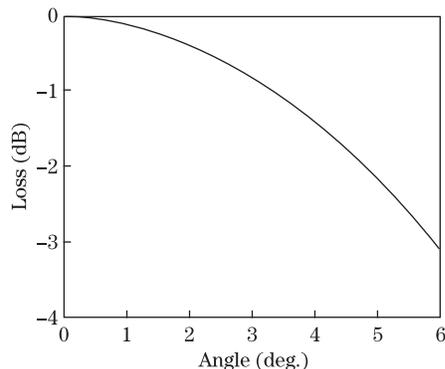


Fig. 3. Excess loss caused by the grating tooth facet angle.

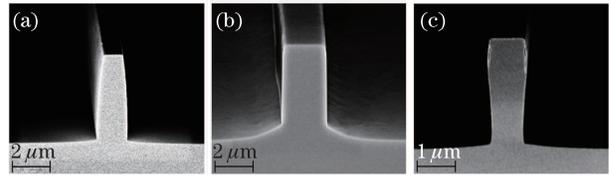


Fig. 4. (a) SEM images of the etched waveguide sidewalls with positive deviation angle using  $\text{CHF}_3$  and  $\text{CF}_4$  fluxes of 6 and 50 sccm, respectively; (b) SEM images of the etched waveguide sidewalls with negative deviation angle using  $\text{CHF}_3$  and  $\text{CF}_4$  fluxes of 40 and 16 sccm, respectively; (c) SEM images of the etched waveguide sidewalls with almost vertical angle using  $\text{CHF}_3$  and  $\text{CF}_4$  fluxes of 20 and 36 sccm, respectively.

developed to form the soft mask for  $\text{SiO}_2$  etching via the contact lithography method. The  $\text{SiO}_2$  film is hydrophobic; thus, the photoresist is often stripped off unexpectedly during the developing process. Several nanometer thick hydrophilic hydrocarbon polymer layers were formed on the  $\text{SiO}_2$  film surface by ICP (Oxford ICP Etching System Plasmalab 100)  $\text{CH}_4$  etching process<sup>[12]</sup>, effectively solving the stripping problem by enhancing the photoresist adherence to the  $\text{SiO}_2$  film.  $\text{CHF}_3$  and  $\text{CF}_4$  gases were used with STS Multiplex ICP to etch the  $\text{SiO}_2$  mask. With the  $\text{SiO}_2$  mask, chromium was etched in Oxford ICP via reaction with chlorine and oxygen radical to form volatile  $\text{CrO}_2\text{Cl}_2$  gas plasma<sup>[13]</sup>. Some deposition caused by the impurity in chromium was distributed along the edge of the etching pattern, which was eliminated by two subsequent continuous ICP processes with chlorine and oxygen radical individually.

$\text{CHF}_3$  and  $\text{CF}_4$  were used as the reaction gases to deep etch  $\text{SiO}_2$  and SiON film anisotropically by STS Multiplex ICP. The anisotropic reacting mechanism is as follows. The negative F ion reacts with  $\text{SiO}_2$  film isotropically, whereas the fluorocarbon film is deposited on the side of the etching pattern, preventing undercut etching and resulting in a balance that determines the sidewall angle.  $\text{CHF}_3$  produces superfluous fluorocarbon film, whereas  $\text{CF}_4$  produces deficient fluorocarbon film<sup>[14]</sup>. Thus, ideally vertical sidewalls are obtained by carefully tuning the flow rates of the two gases. Figure 4 shows the scanning electron microscopy (SEM) images of the sidewall slope angle variation with different  $\text{CHF}_3/\text{CF}_4$  flux ratios. Finally,  $\text{CHF}_3$  and  $\text{CF}_4$  fluxes were set to 20 and 36 sccm, respectively. A 4- $\mu\text{m}$ -deep SiON and  $\text{SiO}_2$  etching was achieved with a sidewall angle of less than  $1^\circ$  from the vertical. The SEM image of the vertical and smooth etched grating teeth is shown in Fig. 5.

Aluminum was coated on the back of the grating facets by lift-off process to increase the reflectivity of the grating teeth. The reflectance of the aluminum-coated facet is 86%. A 6- $\mu\text{m}$ -thick  $\text{SiO}_2$  cover layer was then deposited by PECVD. After dicing, the device with a size of  $11 \times 6$  (mm) was obtained; its microscopic image is shown in Fig. 6.

An external-cavity tunable laser (new focus 6316 velocity laser diode) was used to measure the spectral response of the device. Although the total number of output waveguides is 120, only 56 channels can be measured because of the limitation of the tunable laser, which operates from 838 to 852 nm. TE-polarized light was end-to-end coupled into the input waveguide via a

polarization-maintaining lensed fiber. Another lensed fiber was aligned to the output waveguide to collect the output signal to a photodetector (Newport Model 1931/2931 Series). The transmission spectrum was obtained by scanning the 838- to 852-nm wavelength range and the 56-waveguide channels. Figure 7 shows the measured spectral response, which is normalized with respect to the transmission spectrum of a straight waveguide. The measured channel spacing is 0.24 nm, highly similar to the design value of 0.25 nm. The adjacent channel crosstalk is less than  $-25$  dB. The 3-dB bandwidth is about 0.09 nm. The channel non-uniformity is 3 dB and the insertion loss is 14 dB with respect to the reference straight waveguide. The TM-polarized light transmission spectra were also measured. Compared with the TE-polarized light, a wavelength shift of 0.3 nm, which corresponds to the birefringence of the slab waveguide with an effective refractive index difference of  $9.68 \times 10^{-4}$ , was observed.

Several factors contributed to the relatively large insertion loss of 14 dB. First, the lithography mask used in the contact lithography method has a pixel resolution limit from 50 to 60 nm, which caused sidewall roughness of the waveguides bends. The relation between the loss and the sidewall roughness of a waveguide bend with

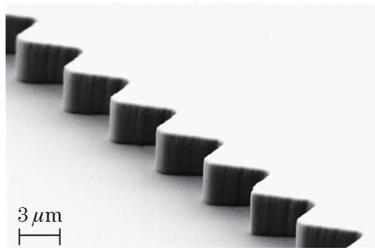


Fig. 5. SEM image of smooth and vertical sidewalls of the grating teeth.



Fig. 6. Microscopic image of the fabricated EDG device.

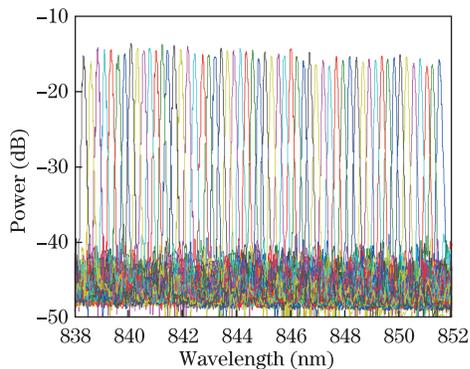


Fig. 7. 56-channel transmission spectrum of the EDG device.

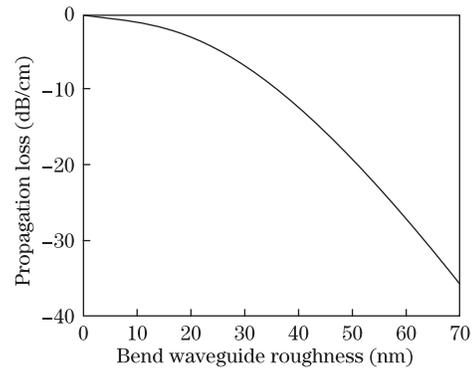


Fig. 8. Propagation loss versus bent waveguide roughness.

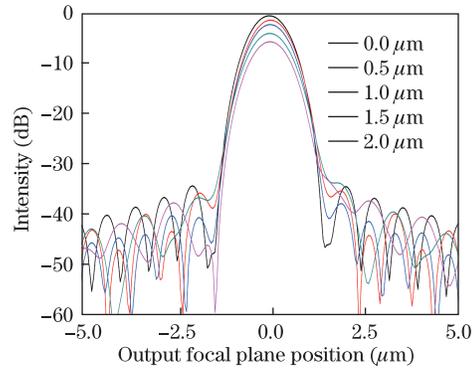


Fig. 9. Light power distribution along the output focal plane of the slab waveguide for different rounding corner radii of the grating teeth.

a bending radius of  $800 \mu\text{m}$  is shown in Fig. 8, which was calculated using the beam propagation method. A sidewall roughness of 60 nm produces about 6 dB of excess loss for the  $2000\text{-}\mu\text{m}$ -long waveguide bend in our device. Another evident effect caused by contact lithography is about  $1 \mu\text{m}$  radius rounding corner of the grating teeth, which results in a 3-dB loss based on the simulation by scalar diffraction method, as shown in Fig. 9. The remaining 5 dB loss can be attributed to the metal reflective coating deficiency, the slab waveguide loss, the grating tooth pattern roughness caused by mask pixel resolution limit, the sidewall roughness, and the loss of diffraction by the grating towards the opposite direction of the slab, among others. Based on the aforementioned analysis, using a higher resolution lithography tool such as the E-beam lithography or stepper is required to reduce the insertion loss.

In conclusion, we present our preliminary experimental results on SiON based EDG spectrometer-on-chip. The ICP deep etching process is developed using chromium hard mask with optimized CHF<sub>3</sub> and CF<sub>4</sub> gas ratio to obtain a vertical and a smooth sidewall. Spectral responses for the 56 channels with a resolution of 0.24 nm in the range from 838 to 852 nm are measured. The chip exhibits positive performance in terms of crosstalk, channel uniformity, and 3-dB bandwidth. The device size is only  $11 \times 6$  (mm). Further improvement of the device is currently in progress, including the reduction of insertion loss, elimination of polarization dependent spectral shift by polarization compensation technique<sup>[15]</sup>, and the integration of silicon photodetectors on the micro-

spectrometer chip.

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