All-optical prefix tree adder with the help of terahertz optical asymmetric demultiplexer

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We propose and describe an all-optical prefix tree adder with the help of a terahertz optical asymmetric demultiplexer (TOAD) using a set of optical switches. The prefix tree adder is useful in compound adder implementation. It is preferred over the ripple carry adder and the carry lookahead adder. We also describe the principle and possibilities of the all-optical prefix tree adder. The theoretical model is presented and verified through numerical simulation. The new method promises higher processing speed and accuracy. The model can be extended for studying more complex all-optical circuits of enhanced functionality in which the prefix tree adder is the basic building block.

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Various architectures, algorithms, and logical and arithmetic operations have been proposed in the field of optical/optoelectronic computing and parallel signal processing in the last decades[1−5]. Ahmed *et al*. have designed a logic unit using a polarization-encoded optical shadow casting scheme[6]. Mukhopadhyay *et al*. have proposed an all-optical arithmetic multiplication scheme with nonlinear material[7]. McAulay has reported an optical arithmetic unit using bit wavelength diviston multiplexer (WDM)[8]. Among the proposed schemes, the terahertz optical asymmetric demultiplexer (TOAD) semiconductor optical amplifier (SOA) assisted Sagnac gate effectively combines fast switching time and reasonable noise figure with the ease of integration and overall practicality that enables it to compete favorably with other similar optical time division multiplexing (OTDM) devices[9−17]. In our previous publication, we have proposed TOAD-based tree architectures for all-optical logic and arithmetic operations[18], all-optical arithmetic units[19], and all-optical adder/subtractor units[20]. The all-optical prefix tree adder has many potential applications in optical computing. In this letter, we propose and describe the TOAD-based switch as basis for designing an integrated circuit which can perform the addition of two 2-bit numbers in an all-optical domain. Simulation of the proposed design has also been conducted with the help of Matlab-6.5.

In recent years, the TOAD-based gate has taken an important role in optical communication and information processing[21−27]. Sokoloff *et al*. have demonstrated a new device, a TOAD capable of demultiplexing data at 50 Gb/s[3]. The TOAD consists of a loop mirror with an additional intra-loop 2×2 (ideally 50:50) coupler. The loop contains a control pulse whose light is different from that of an incoming pulse and a SOA that is offset from the loop's midpoint by a distance Δx (Fig. 1). In our earlier paper, we have tried to utilize the output from both the transmitting and reflecting modes of the device[19−23] to perform logical and arithmetic operations. In this letter, we utilize the same procedure.

The output powers at ports 1 and 2 can be expressed as[28−30]

$$P_{\rm out}(t) = \frac{P_{\rm in}(t)}{4} \cdot \{G_{\rm cw}(t) + G_{\rm ccw}(t) \mp 2\sqrt{G_{\rm cw}(t) \cdot G_{\rm ccw}(t)} \cdot \cos(\Delta\varphi)\}, \quad (1)$$

where $G_{\rm cw}(t)$ and $G_{\rm ccw}(t)$ are the power gains for clockwise (cw) and counter clockwise (ccw) pulses. The time-dependent phase difference between cw and ccw pulses is[28]

$$\Delta\varphi = -\alpha/2 \cdot \ln[G_{\rm cw}(t)/G_{\rm ccw}(t)] \quad (2)$$

with α being the line width enhancement factor. When a

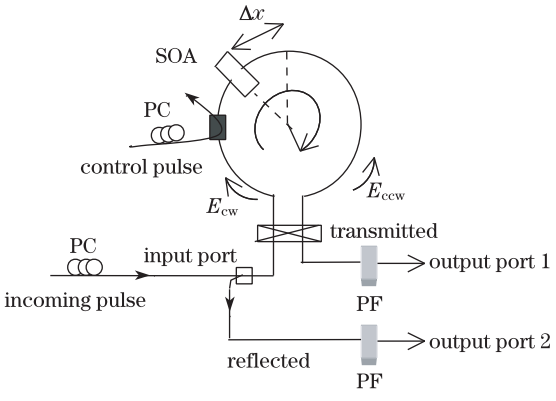

Fig. 1. TOAD-based optical switch. PC: polarization controller; PF: polarization filter; $E_{\rm cw}$: clockwise electric field; $E_{\rm ccw}$: counter clockwise electric field.

control pulse is injected into the loop, it saturates the SOA and changes its refraction index. The SOA gain decreases rapidly according to[2,28]

$$G(t) = \frac{1}{1-(1-\frac{1}{G_{\rm ss}})\exp\left(-\frac{E_{\rm cp}(t)}{E_{\rm sat}}\right)}, \quad t \leqslant t_{\rm s}, \qquad (3)$$

where $G_{\rm ss}$ stands for small signal gain, $E_{\rm sat}$ is the saturation energy of the SOA, $t_{\rm s}$ is the saturation time of SOA and $E_{\rm cp}(t) = \int_{\infty}^{t} P_{\rm cp}(t'){\rm d}t'$. In this letter, we consider Gaussian pulse $P_{\rm cp}(t) = \frac{E_{\rm cp}}{\sigma\sqrt{\pi}}\exp\left(-\frac{t^2}{\sigma^2}\right)$ as the control signal, where $E_{\rm cp}$ is the control pulse energy and σ is the full-width at half-maximum (FWHM). After a while, the gain recovers due to the injection of carriers and can be obtained from the gain recovery formula[1,29]:

$$G(t) = G_{\rm ss}\left[\frac{G(t_{\rm s})}{G_{\rm ss}}\right]^{\exp\left[-\frac{(t-t_{\rm s}}{\tau_{\rm e}}\right]}, \quad t \geqslant t_{\rm s}, \qquad (4)$$

where $\tau_{\rm e}$ is the gain recovery time. As a result, the two counter-propagation data signals experience different gain saturation profiles, i.e., $G_{\rm ccw} \neq G_{\rm cw}$. Therefore, the signals recombine at the input coupler. When $\Delta\varphi \approx \pi$, the data will exit from output port 1, i.e., $P_{\rm out,1}(t) \neq 0$ and $P_{\rm out,2}(t) \approx 0$. Subsequently, the corresponding values can be obtained from Eq. (1). The energy of the control pulse is 10 times greater than that of the incoming pulse. The control pulse and incoming pulse can be discriminated by appropriately adjusting their polarization states using polarization controllers (PCs) so that they are orthogonal to each other. The output of any switch can be used as an incoming/control pulse for the other provided that they pass through a variable optical attenuator and a PC. A polarization beam splitter (PBS) may be used at the output of the TOAD-based switch to reject the control pulse and pass the incoming pulse. The block diagram is shown in Fig. 2.

In the absence of a control signal, the incoming pulse clearly exits through the reflecting port of TOAD which can be separated by optical circulator and reaches the output port 2.In this case, no light is present in output port 1. However, in the presence of the control signal, the incoming signal exits through the transmitting port of TOAD and reaches the output port 1. In this case, no light is present in the output port 2. In the absence of the incoming signal, ports 1 and 2 receive no light because the filter blocks the control signal. Schares *et al*. have shown that when amplified spontaneous emission (ASE) becomes high enough, it influences the gain saturation only when SOA is longer than 150 μm[30].

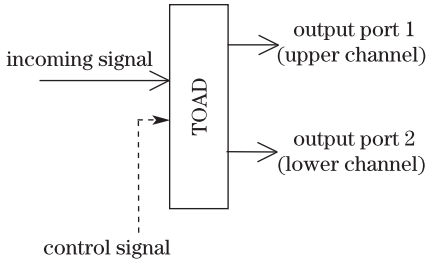

Fig. 2. Schematic diagram of TOAD-based optical switch.

The control pulse energy is much lower than 1 pJ and the pulse width is narrow. Thus, two-photon absorption (TPA) and ultrafast nonlinear refraction (UNR) are neglected[31]. The SOA length is smaller than 150 μm. In different stages, we use an optical attenuator such that every TOAD gets the same input intensity. We also use control and incoming signals that are of different orthogonal polarizations. Hence, cascading is not difficult. No additional input light source is used in any stage; hence, no synchronization problem is observed in higher bit arithmetic[32].

In the adder circuit, the carry propagation delay is the major concern when we try to speed up the addition of any two numbers. For an n-bit ripple carry adder, the delay time is linear to n. This happens due to the carry propagation from the least significant bit position to the most significant bit (MSB) position. This represents the time we need to wait in relation to the worst case for the full adder in MSB position to produce the correct "sum" and "carry out". The prefix trees are interconnected such that carry signals are computed partially in parallel. The carry signal computed in an initial stage of a given prefix tree is used in subsequent stages of the given prefix tree without introducing additional delay in the computation of other carry signals in other prefix trees associated with higher bit positions. In the prefix tree, the outputs of the block are labeled with a pair of integers corresponding to the initial and the final bit that is spanned by the output. For n power-of-two, the number of levels is $L = \log_2(n) + 1$ because each level produces a double of the bits spanned. The expression for the delay is $t_{\rm a,g} + \log_2(n)t_{\rm block} + t_{\rm XOR}$, where $t_{\rm a,g}$ stands for delay in computing generate (g) and alive (a), $t_{\rm block}$ stands for the total block delay, and $t_{\rm XOR}$ stands for the delay in computing XOR operation. The number of blocks is $(n/2)\log_2(n) + 1$ because each level (except the last) has $n/2$ blocks.

In general, we can accomplish a prefix combinational network of n inputs by computing

$$\left.\begin{aligned} g_i &= x_i \cdot y_i \\ p_i &= x_i \oplus y_i \\ a_i &= x_i + y_i \end{aligned}\right\}, \qquad (5)$$

$$F_i = g_i + a_i \cdot C_{i-1}, \qquad (6)$$

$$S_i = p_i \oplus C_{i-1}. \qquad (7)$$

Here, the different signals are propagate (p), generate (g). and alive (a). Sum (S) gives the resulting sum and C_{i-1} is the carry-over from the previous stage. Equation (6) is implemented with the help of the GPA (generate, propagate, and alive) block.

We use three TOAD-based switches for designing an all-optical GPA block (Block-1) as shown in Fig. 3(a). This block is used to produce three signals, i.e., p, g, and a. The output terminals T_1, T_2, T_3, and T_4 produce the logic operation $\overline{x_i}y_i$, x_iy_i, $x_i\overline{y_i}$, and x_iy_i, respectively. According to the operation principle of the TOAD-based switch, g_i takes the expression $x_i{\cdot}y_i$. The outputs of T_1 and T_3 combine to produce p_i. Thus, p_i takes the expression $x_i{\oplus}y_i$. Again, g_i and p_i combine with the help of the beam combiner (BC) to produce a_i.

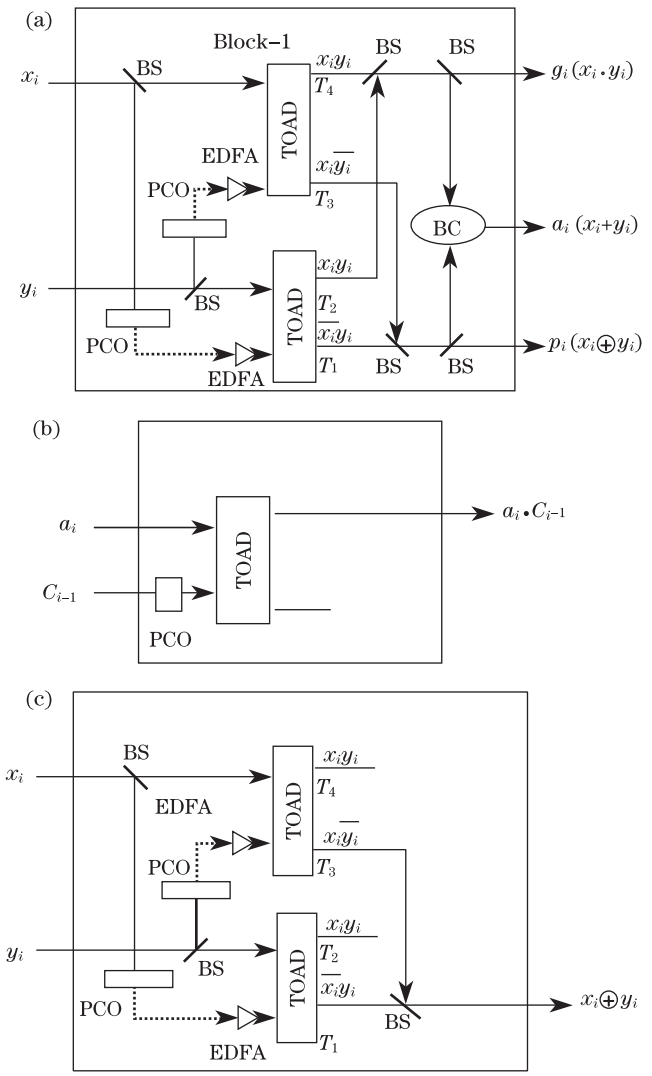

Fig. 3. (a) All-optical circuit to compute GPA; (b) all-optical AND gate; (c) all-optical XOR gate. BS: beam splitter.

Light from input "x_i" and "y_i" is directly connected to TOAD-based switches to act as incoming signals. The inputs "x_i" and "y_i" are also connected to switches through polarization converter (PCO) and erbium doped fiber amplifier (EDFA), so they can act as control signals (Fig. 3(a)). The Jones matrix of the PCO ($\lambda/2$ plate with azimuth angle θ of the optical axis) is $M_{\lambda/2}(\theta) = \begin{pmatrix} \cos 2\theta & \sin 2\theta \\ \sin 2\theta & -\cos 2\theta \end{pmatrix}$. Here, we choose $\theta = 45°$, such that vertically polarized light converts into horizontal light and *vice versa* when light passes. Hence, the control and incoming pulses can be converted to two types of orthogonally polarized light.

The optical circuit diagram for AND gate is shown in Fig. 3(b). Optical XOR gate is shown in Fig. 3(c).

We use two GPA blocks (i.e., Block-1(a) and 1(b)), two AND gates, and two XOR gates to design a two-bit all-optical prefix tree adder (Fig. 4). The developed model can handle arbitrary data patterns $X(x_1x_0)$ and $Y(y_1y_0)$.

Let us consider an example where $X = 11$ (x_1x_0), $Y = 10$ (y_1y_0), and the carry input $C_{\rm in} = 1$. In Block-1(a), the two inputs are $x_0 = 1$ and $y_0 = 0$. Thus, according

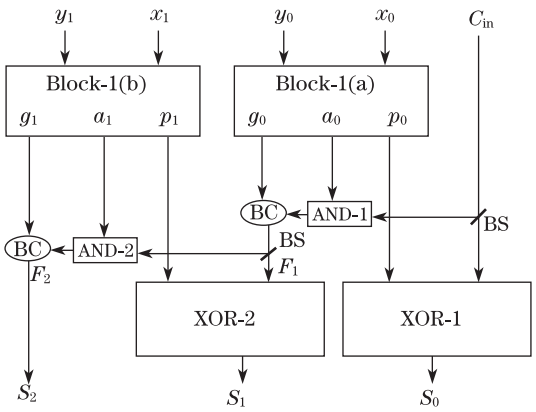

Fig. 4. All-optical prefix tree adder.

to the operational principle of Block-1, three outputs are generated as $p_0 = 1$, $g_0 = 0$, and $a_0 = 1$. Again, in XOR-1, the two inputs receive the values 1 and 1 (as p_0 of Block-1(a) directly connect to one input of XOR-1 and carry from the previous stage $C_{\rm in} = 1$). It generates the output $S_0 = 0$ (as $p_0 = 0$). In AND-1, it receives the two inputs as 1 and 1, as a_0 of Block-1(a) is one, and $C_{\rm in}$ from previous is also carried over as 1; and the output is produced as 1. The outputs of AND-1 and g_0 are combined with the help of BC to produce F_1. Thus, $F_1 = 1$. In Block-1(b), the two inputs are $x_1 = 1$ and $y_1 = 1$. Consequently, it will produce the three outputs as $p_1 = 0$, $g_1 = 1$, and $a_1 = 1$. Similarly, two inputs are received by XOR-2 as 0 and 1 (as $p_1 = 0$ and $F_1 = 1$). Hence, it will generate the output of $S_1 = 1$. In AND-2, it receives two inputs 1 and 1 (as $a_1 = 1$ and $F_1 = 1$) and generates the output as 1. Lastly, g_1 and the output of AND-2 are combined to produce one output, i.e., $F_2 = 1$. As S_2 takes the same value as F_2, then $S_2 = 1$. The final output is 110 ($S_2S_1S_0$), which verifies the addition of two 2-bit input numbers. The truth table of this prefix tree adder is shown in Table 1.

The different parameters used in simulation have been taken from literature that reports experimental results[7,28,29,33]. For this simulation, we choose the following parameters: $G_{\rm ss} = 20$ dB, $\alpha = 6$, $\tau_{\rm e} = 50$ ps, full-width at half-maximum (FWHM) of control pulse $T_{\rm FWHM} = 3.33$ ps, eccentricity of the loop $T = 30$ ps, and control energy of 70 fJ. The developed model can handle arbitrary data patterns $X(x_1x_0)$ and $Y(y_1y_0)$. Let us consider for example three sets of inputs, where $X = 11, 10, 01$, $Y = 10, 11, 10$, and $C_{\rm in} = 1, 0, 1$. The corresponding output waveforms are shown in Fig. 5.

We select the output extinction ratio (ER) as the optimization criterion, which indicates the opening of the eye diagram. It is defined as

$$\mathrm{ER} = 10\ \log\left(\frac{P^1_{\rm min}}{P^0_{\rm max}}\right), \tag{8}$$

where $P^1_{\rm min}$ and $P^0_{\rm max}$ are the minimum and maximum values of the peak power of "1" and "0", respectively. From Eq. (8), we can calculate the output ER (dB) for prefix tree adder. It has the value of 39.99 dB. Figure 6 shows the variation of ER with control pulse energy ($E_{\rm cp}$) when the eccentricity of the loop (T) is kept constant. The maximum ER is obtained at 70-fJ control pulse

Table 1. Truth Table of the Prefix Tree Adder

Input X	Input Y	Carry Input	Output S
x_1 x_0	y_1 y_0	C_{in}	$S_2S_1S_0$
1 1	1 0	1	110
1 0	1 1	0	101
0 1	1 0	1	100

energy. The ER increases rapidly and then decreases after E_{cp} reaches 70 fJ. Figure 7 shows the variation of ER with gain recovery time τ_{e} other parameters are kept constant. The maximum ER is obtained at about 50 ps. When the gain recovery time increases, the corresponding ER values decreases. Figure 7 also shows that when $\tau_{\text{e}} = 70$, 80, and 90 ps, the corresponding ER values are about 29.67, 23.32, and 19.12 dB, respectively.

Figure 8 shows the variation of ER with T when E_{cp} is constant. This confirms that ER is high when the eccentricity loop T is 30 ps.

The quality factor Q of this circuit (Fig. 4) can be expressed as[2]

$$Q = \frac{P_1 - P_0}{\sigma_1 + \sigma_0}, \tag{9}$$

where P_1 (P_0) and σ_1 (σ_0) are the average power and standard deviation of the circuit outputs at high state (0 state), respectively. Bit error rate (BER) is likewise obtained from

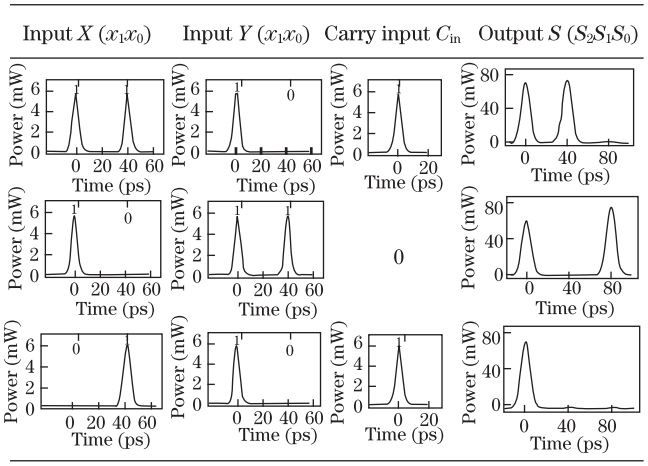

Fig. 5. Simulated waveforms of the prefix tree adder.

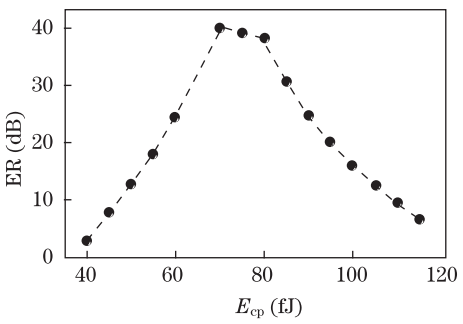

Fig. 6. Variation of ER with control pulse energy E_{cp}.

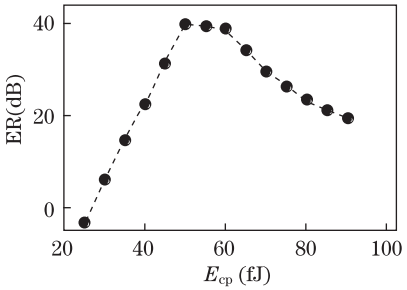

Fig. 7. Variation of ER with gain recovery time τ_{e}.

$$\text{BER} = \frac{1}{2}\text{erfc}\left(\frac{Q}{\sqrt{2}}\right) = \frac{\exp\left(\frac{-Q^2}{2}\right)}{Q\sqrt{2\pi}}, \tag{10}$$

where erfc is the complimentary error function. We obtain the output data by varying the input as $0 \to 0$, $0 \to 1$, $1 \to 1$, $1 \to 0$, etc. It is estimated that thousands of data are simulated by the computer to calculate the BER. We also plot BER against different values of control pulse energy E_{cp}. The results are shown in Fig. 9.

Using the operation conditions, we obtain the ER and BER at 39.99 dB and nearly 10^{-13}, respectively, which are adequate for all-optical logic applications. The performance of this circuit depends on SOA carrier lifetime. This parameter is crucial and can impose a strict limitation on the gate performance, which can severely alter the pattern effect observed on the switched-out pulses. Hence, carrier lifetime should be reduced. The most direct method to achieve this goal is increasing SOA injection current and length[34], but the cost increases

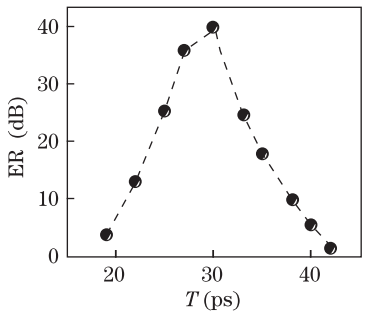

Fig. 8. Variation of ER with the eccentricity of the loop T of TOAD.

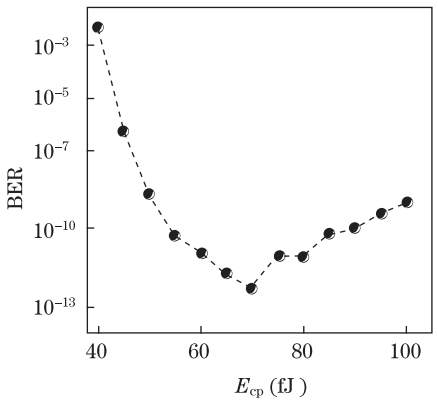

Fig. 9. Variation of BER with control pulse energy E_{cp}.

twofold[14]. As the SOA length increases, we cannot neglect ASE[35]. Moreover, quantum dot SOAs can be used for complex gain recovery enhancement technology to reduce carrier lifetime[36]. Recently, high-speed operations have been successfully demonstrated using a hybrid-integrated Mach-Zehnder interferometer (MZI) all-optical switch, which can demultiplex 168-Gb/s data pulse[37]. Similarly, 320-Gb/s operations have been successfully reported[38]. Our proposed prefix tree adder is also applicable when using a SOA-MZI-based switch.

In conclusion, the significant advantage in the proposed design is that the proposed prefix tree adder can perform addition operations, which are all-optical in nature. This scheme can be extended and implemented easily and successfully for any higher number of input digits by the proper incorporation of TOAD-based switches. Numerical simulation results confirming the described method are provided. In our proposed design, we achieve the ER and BER of 39.99 dB and nearly 10^{-13}, respectively, which are adequate for all-optical logic applications.

References

1. G. Li, F. Qian, H. Ruan, and L. Liu, Appl. Opt. **38,** 5039 (1999).
2. G. P. Agrawal, *Applications of Nonlinear Fibre Optics* (Academic, San Diego 2001).
3. J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, IEEE Photon. Technol. Lett. **5,** 787 (1993).
4. Z. Y. Shen and L. L. Wu, Appl. Opt. **47,** 3737 (2008).
5. K. E. Zoiros, T. Houbavlis, and M. Kalyvas, Opt. Quantum Electron. **36,** 1005 (2004).
6. J. U. Ahmed and A. A. S. Awwal, in *Proceedings of IEEE Aerospace and Electronics Conference* **3,** 1146 (1992).
7. S. Mukhopadhyay, D. N. Das, P. P. Das, and P. Ghosh, Opt. Eng. **40,** 1998 (2001).
8. A. D. McAulay, Opt. Laser Technol. **32,** 421 (2000).
9. R. Ramaswami and K. N. Sivarajan, *Optical Networks: A Practical Perspective* (Morgan Kaufmann Publishers, San Francisco, 2001)
10. S. Zhang, D. Lenstra, Y. Liu, H. Ju, Z. Li, G. D. Khoe, and H. J. S. Dorren, Opt. Commun. **270,** 85 (2007).
11. K. Huybrechts, G. Morthier, and R. Baets, Opt. Express **16,** 11405 (2008).
12. Y. Ueno, Opt. Commun. **229,** 253 (2004).
13. V. M. Menon, W. Tong, C. Li, F. Xia, I. Glesk, P. R. Prucnal, and S. R. Forrest, IEEE Photon. Technol. Lett. **15,** 254 (2003).
14. K. E. Zoiros, G. Papadopoulos, T. Houbavlis, and G. T. Kanellos, Opt. Commun. **258,** 114 (2006).
15. B. Dagens, A. Labrousse, R. Brenot, B. Lavigne, and M. Renaud, in *Proceedings of OFC 2003* ThX1 (2003).
16. I. Glesk, R. J. Runser, and P. R. Prucnal, Acta Phys. Slov. **51,** 151 (2001).
17. K. E. Zoiros, J. Vardakas, T. Houbavlis, and M. Moyssidis, Optik **116,** 527 (2005).
18. J. N. Roy and D. K. Gayen, Appl. Opt. **46,** 5304 (2007).
19. D. K. Gayen and J. N. Roy, Appl. Opt. **47,** 933 (2008).
20. D. K. Gayen, R. K. Pal, and J. N. Roy, Chin. Opt. Lett. **7,** 530 (2009).
21. T. Chattopadhyay and J. N. Roy, Optik **121,** 617 (2010).
22. T. Chattopadhyay, C. Taraphdar, and J. N. Roy, Appl. Opt. **42,** E35 (2009).
23. T. Chattopadhyay, J. N. Roy, and A. K. Chakraborty, Opt. Commun. **282,** 1287 (2009).
24. T. Houbavlis and K. E. Zoiros, Opt. Eng. **42,** 3415 (2003).
25. J. P. Sokoloff, I. Glesk, P. R. Prucnal, and R. K. Boneck, IEEE Photon. Technol. Lett. **6,** 98 (1994).
26. K. E. Zoiros, R. Chasioti, C. S. Koukourlis, and T. Houbavlis, Optik **118,** 134 (2007).
27. T. Houbavlis and K. E. Zoiros, Opt. Quantum Electron. **35,** 1175 (2003).
28. M. Eiselt, W. Pieper, and H. G. Weber, J. Lightwave Technol. **13,** 2099 (1995).
29. K. I. Kang, T. G. Chang, I. Glesk, and P. R. Prucnal, Appl. Opt. **35**, 417 (1996).
30. L. Schares, C. Schubert, C. Schmidt, H. G. Weber, L. Occhi, and G. Guekos, IEEE J. Quantum Electron. **39,** 1394 (2003).
31. J. M. Tang and K. A. Shore, IEEE J. Quantum Electron. **34,** 1263 (1998).
32. T. Chattopadhyay, "Eliminating the additional input beam in all-optical XOR gate using terahertz optical asymmetric demultiplexer (TOAD) based interferometer: a theoretical analysis", Optik International Journal for Light and Electron Optics (in press), doi:10.1016/j.ijleo.2010.09.033.
33. Y. K. Huang, I. Glesk, R. Shankar, and P. R. Prucnal, Opt. Express **14,** 10339 (2006).
34. F. Girardin, G. Guekos, and A. Houbavlis, IEEE Photon. Technol. Lett. **10,** 784 (1998).
35. L. Schares, C. Schubert, C. Schmidt, H. G. Weber, L. Occhi, and G. Guekos, IEEE J. Quantum Electron. **39,** 1394 (2003).
36. Y. Kitagawa, N. Ozaki, Y. Takata, N. Ikeda, Y. Watanabe, Y. Sugimoto, and K. Asakawa, J. Lightwave Technol. **27,** 1241 (2009).
37. S. Nakamura, Y. Ueno, and K. Tajima, IEEE Photon. Technol. Lett. **13,** 1091 (2001).
38. Y. Liu, E. Tangdiongea, Z. Li, H. de Waardt, A. M. J. Koonen, G. D. Khoe, X. Shu, I. Bennion, and H. J. S. Dorren, J. Lightwave Technol. **25,** 103 (2007).